T.E. ETRX VI (Rev)
Elective I - Computer org.1

Con. 3242-11. (REVISED COURSE) RK-2625

(3 Hours) [Total Marks : 100

N.B. (1) Question No. **1** is **compulsory**.
(2) **All** questions carry **equal** marks.
(3) Solve any **four** from remaining **six**.

1. (a) What is bus Arbitration ? 5
   (b) What is meant by TLB ? 5
   (c) Write Algorithm for multiplication. 5
   (d) Microprogram for $R_1+R_2 \rightarrow R_3$. 5

2. (a) With the help of dual bus structure explain how Data will be Read from memory. The address where Data is present in the memory is in register R_1. The opcode is available in register R_2. 20
   (b) Give the special features of super scalar Architecture.

3. (a) Explain different types of hazards. 20
   (b) Explain how virtual memory concept is implemented between secondary memory, main memory, cache memory and CPU.

4. (a) For five instructions show how four stage pipe line will work. Give the number of 7 states for pipeline and nonpipeline mode. 20
   (b) Explain cache Architecture in detail.

5. (a) Explain ARM family Architecture. 20
   (b) Draw and explain the working of magnetic hard disk.

6. (a) Explain different types of buses used in computer communication. 20
   (b) Explain Addressing modes of intel 32 Architecture.

7. Write short notes on any **two** :— 20
   (a) Hardwired Control Unit.
   (b) Cache replacement policies
   (c) Logical instructions of ARM.